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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,384	09/30/2003	Li-Jau Yang	CISCP584/334845	9157

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Weaver Austin Villeneuve & Sampson LLP
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
PALIWAL, YOGESH	

ART UNIT	PAPER NUMBER
2435	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/676,384	YANG ET AL.	
	Examiner	Art Unit	
	YOGESH PALIWAL	2435	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,7-11,13 and 17-26* is/are pending in the application.

4a) Of the above claim(s) *3,13 and 21-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 7-11, and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Applicant's submission for RCE filed on 10/18/2008 has been entered. Applicant has amended claims 1, 8, 10, 11 and 20; canceled claims 2, 4-6, 12 and 14-16 and added claims 21-26. Currently claims 1, 3, 7-11, 13 and 17-26 are pending in this application of which claims 3, 13, and 21-26 are withdrawn from consideration. The amendment submitted on 10/18/2008 was subjected to restriction and/ election requirement (see, office action dated 01/07/2009). Applicant submitted response to election/restriction on 1/23/2009.

Election/Restrictions

1. Claims 21-26 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 1/23/2009. Applicant's election with traverse of species 1 in the reply is acknowledged. The traversal is on the ground(s) that examiner did not provide explanation to establish the burden. This is not found persuasive because there is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics. The species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search queries); and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph. Fig. 6a (defined

by claims 21-26), describes mutually exclusive design of an apparatus when compared to fig. 6c (defined by claim 11) and 6e (defined by claim 1). Please note that even though claims 1 and 11 are drawn to different figures, based on the current language, examiner feels that language of claims 1 and 11 overlap a lot and the differences are obvious between these two embodiments. However this is not a case with Fig. 6a which requires simply opposite configuration from fig. 6e. For example, in fig. 6a PHY communication module is configured to provide connectivity through a MDIO/MDC interface and PHY controls the operation of crypto device and in fig. 6e, PHY communication module is configured to provide connectivity through a MDIO/MDC interface and PHY controls the operation of crypto device. There is a search burden due to mutually exclusive design of species 2. In order to search for the prior art, examiner would need to search for 2 separate apparatus designs which would require employing different search queries. Moreover, due the mutually exclusive design of each of these species, it is likely that the prior art applicable to one species would not likely be applicable to another species. Therefore, there is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 11, and 17-20 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Please note that in reply filed on 10/18/2008, applicant pointed to Fig. 6c for the support for claim 11. Currently claim 11 recites, crypto engine means coupled to said digital circuitry means and comprising both PHY logic and security logic. Looking at fig. 6c, it appears that applicant is referring to numeral 600 as being the claimed crypto engine means. Claim 11 further recites "wherein said MDIO/MDC interface is configured for controlling both the PHY and the crypto engine means". Fig. 6c does not support such a language and instead Fig. 6c shows that MDIO/MDC interface is configured for controlling both the PHY logic and the security logic. This will be assumed for the examination purposes.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 7-11, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, hereinafter AAPA in view of Dhir et al. (US 2005/0084076 A1), hereinafter "Dhir" and further in view of Buer et al. (US 2004/0139313 A1), hereinafter, "Buer".

Regarding **Claim 1**, AAPA discloses an apparatus comprising:

analog circuitry (see, Fig. 1, Numeral 130) configured to transmit to, and receive data from, a data transmission medium (see, Fig. 1, Numeral 120);

digital circuitry (see, Fig. 1, Numeral 140) directly coupled to said analog circuitry, said digital circuitry configured to transmit data/control signals to, and receive data/control signals from, a Media Access Controller (MAC) (see, Fig. 1, Numerals 140, 160 and 110);

a PHY communications module coupled to said analog and digital circuitry (see, Fig. 1, Numeral 150);

AAPA does not disclose a crypto engine coupled to a digital circuitry; a crypto communication module directly coupled to said crypto engine and an interface link operatively coupling a PHY communication module to a crypto communications module.

Dhir discloses a crypto engine coupled to a digital circuitry (see, Fig. 8, Numeral 321); a crypto communication module directly coupled to said crypto engine (see, Fig. 8, Numeral 321 and 312, and also see, Paragraph 0051, "Accordingly, program memory 312 comprises programming instructions 398 for FPGA 300 to configure encryption engine 321 for either of at least these two types of encryptions being employed, namely, RC4 and DES or triple DES with respect to HiperLAN2.", and also refer to Paragraph 0050, "Memory controller 314 may be programmed using a portion of program instruction 398 for programming programmable gates of FPGA 300 or may be hardwired or embedded with FPGA 300") and an interface link (See, Fig. 8, Numeral

320) operatively coupling a PHY communication module (Fig. 8, Numeral 315) to a crypto communications module (Fig. 8, Numeral 312).

Therefore, it would have been obvious at the time the invention was made to one of ordinary skill in the art to include in the circuitry of AAPA, encryption engine and encryption communication module as taught by Dhir to provide built in security for data passing through the MAC.

The combination of AAPA and Dhir does not explicitly discloses said crypto communication module configured provide direct connectivity through a MDIO/MDC interface and wherein the crypto communication module is further configured to provide control signal to said PHY communication module via said interface link.

However, Buer discloses crypto communication module configured provide direct connectivity through a MDIO/MDC interface (see, Paragraph 0164, "The control provided by the MDC/MDIO interface may be used to configure the security processor during WakeOnLan mode") and wherein the crypto communication module is further configured to provide control signal to said PHY communication module via an interface link (see, Paragraph 0164, "The security processor 1912 provides the link status of the line side SERDES 1928 to the host via a side band link 1920. When the LOW_PWR# input pin 1930 is tied to zero the security processor 1912 exits reset in a low power state.").

Therefore, it would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the design of the combined system of AAPA and Dhir such that crypto communication module configured provide direct connectivity

through a MDIO/MDC interface and wherein the crypto communication module is further configured to provide control signal to said PHY communication module via said interface link as taught by Buer because MDIO/MDC interface is well-known to provide an option to change configuration information during operation, as well as read the PHY's status.

Regarding **Claim 11**, AAPA discloses an apparatus comprising:

analog circuitry means (see, Fig. 1, Numeral 130) configured to transmit to, and receive data from, a data transmission medium (see, Fig. 1, Numeral 120);

digital circuitry means (see, Fig. 1, Numeral 140) coupled to said analog circuitry, said digital circuitry configured to transmit data/control signals to, and receive data/control signals from, a Media Access Controller (MAC) (see, Fig. 1, Numerals 140, 160 and 110);

a PHY communications means coupled to said analog and digital circuitry means, said PHY communication means configured to provide connectivity through an MDIO/MDC interface (see, Fig. 1, Numeral 150);

AAPA further discloses MDIO/MDC interface is configured to control the PHY (see, Fig. 1, Numeral 150).

AAPA does not disclose a crypto engine means coupled to a digital circuitry means; a crypto communication module directly coupled to said crypto engine and an interface link operatively coupling a PHY communication module to a crypto communications module.

Dhir discloses a crypto engine means coupled to a digital circuitry (see, Fig. 8, Numeral 321); a crypto communication module directly coupled to said crypto engine (see, Fig. 8, Numeral 321 and 312, and also see, Paragraph 0051, "Accordingly, program memory 312 comprises programming instructions 398 for FPGA 300 to configure encryption engine 321 for either of at least these two types of encryptions being employed, namely, RC4 and DES or triple DES with respect to HiperLAN2.", and also refer to Paragraph 0050, "Memory controller 314 may be programmed using a portion of program instruction 398 for programming programmable gates of FPGA 300 or may be hardwired or embedded with FPGA 300") and an interface link (See, Fig. 8, Numeral 320) operatively coupling a PHY communication module (Fig. 8, Numeral 315) to a crypto communications module (Fig. 8, Numeral 312).

Therefore, it would have been obvious at the time the invention was made to one of ordinary skill in the art to include in the circuitry of AAPA, encryption engine and encryption communication module as taught by Dhir to provide built in security for data passing through the MAC.

The combination of AAPA and Dhir does not explicitly discloses a crypto engine means comprising both PHY logic and security logic and said crypto communications means coupled to said MDIO/MDC interface, wherein said MDIO/MDC interface is configured for the crypto engine means.

However, Buer discloses a crypto engine means comprising both PHY logic and security logic (see, Fig. 5, Numeral 312) and said crypto communications means coupled to said MDIO/MDC interface, wherein said MDIO/MDC interface is configured

for the security logic see, Paragraph 0164, "The control provided by the MDC/MDIO interface may be used to configure the security processor during WakeOnLan mode").

Therefore, it would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the design of the combined system of AAPA and Dhir such crypto engine means comprising both PHY logic and security logic and said crypto communications means coupled to said MDIO/MDC interface, wherein said MDIO/MDC interface is configured for the crypto engine means as taught by Buer because MDIO/MDC interface is well-known to provide an option to change configuration information during operation, as well as read the PHY's status.

Regarding **Claims 7 and 17**, the rejection of claims 1 and 11 is incorporated and the combination of AAPA, Dhir and Buer further discloses that PHY communications module is configured to provide connectivity through a communication medium (see AAPA, Fig. 1, Numeral 120 and see Dhir Fig. 8, Numerals 301 and 312, WLAN transceiver is connected to program memory 312)

Regarding **Claims 8 and 18**, the rejection of claims 7 and 17 is incorporated and the combination of AAPA, Dhir and Buer further discloses that said communication medium is configured to communicate with a plurality of devices (See Dhir, Paragraphs 0044 and 45)

Regarding **Claims 9 and 19**, the rejection of claims 8 and 18 is incorporated and the combination of AAPA, Dhir and Buer further discloses that plurality of devices include at least one device that communicates at the PHY level (see Dhir, Paragraph

0045, "baseband processor 324"), and at least one device that performs both PHY and security functions (Dhir, Paragraph 0045, "encryption engine").

Regarding **Claims 10 and 20**, the rejection of claims 7 and 17 is incorporated and the combination of AAPA, Dhir and Buer further discloses that said communication medium communicates with at least one device that performs both PHY and Security functions (see Dhir, Paragraph 0045, "encryption engine 321").

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOGESH PALIWAL whose telephone number is (571)270-1807. The examiner can normally be reached on M-F: 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on (571) 272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Y. P./
Examiner, Art Unit 2435

/Kimyen Vu/

Supervisory Patent Examiner, Art Unit 2435